Guillem López Paradís

Senior Research Scientist • Computer Architecture & Hyperscale

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Short Bio

Guillem is a **Computer Architecture Researcher** with a **PhD from BSC-UPC (2025 - Cum Laude)**. As a research lead specialising in **RTL simulation scalability**, coherent memory systems, and **scalable MPMC queue-based communication** for accelerators, he has a proven track record of architecting high-impact data movement solutions for **hyperscale environments**, achieving **>100× speedups** in data transfer. An expert in hardware-software co-design, he is currently leading research into **LLM-based**, agent-driven **workflows** to **automate hardware design**, including RTL generation and architectural exploration. Guillem has a history of **leading international collaborations** with **Arm, UCSB, and PoliMilano** and mentoring talent as a **Google Summer of Code Mentor**. His research is published at premier venues including **ISCA, DATE, and ICPP**, and he is an active leader in the architecture community, serving on the **Program Committees for ISCA, MICRO, CF** and the **ASPLOS and ISCA AEC**.

Education

PhD in Computer Architecture

May 2021 – July 2025

Polytechnic University of Catalonia (UPC) *Cum Laude*

- Thesis: *Efficient Data Movement in Large-Scale Heterogeneous Systems*
- Advisors: Prof. **Adrià Armejach** & Prof. **Miquel Moretó**. Collaborators: Prof. **Jonathan Balkind** (UCSB) & Dr. Balaji Venu (Arm).
- **Key Outcomes**: Published at **ISCA '24** (co-first author) and multiple papers at **DATE** and **ICPP**.
- Architected the **Data Centre HyperLoops (DHL)**, **Metro-MPI** simulation framework, and scalable accelerator communication patterns.
- **Funding**: Secured **€107,000** in competitive research funding, including the **FI** and **NGI Fellowships**.

Visiting Scholar (Short-Term Scholar / NGI Fellow)

Oct '23 – Feb '24 | Nov '24 – May '25

University of California, Santa Barbara (UCSB) *Santa Barbara, USA*

- **Research Leadership**: Led a multidisciplinary group of 6 researchers (PhD, Master, and Undergrads).
- **Impact**: Co-developed **Data Centre HyperLoops** (DHL), a solution for efficient inter-chip communications.
- *Received the **NGI Fellowship** (€25,000), the Severo Ochoa grant (€3,500), and the **FI Mobility** grant (€3,000).*

MSc in Innovation and Research in Informatics

Feb 2018 – Nov 2020

Polytechnic University of Catalonia (UPC) · Specialisation in High-Performance Computing (HPC) *GPA: 8.9/10*

BSc Mobility Exchange

Feb 2017 – July 2017

École Polytechnique Fédérale de Lausanne (EPFL) *GPA: 5/6*

- Achieved **Honours in Embedded Systems** by designing an **RTL sorting accelerator with >10× speedup**; awarded **Swiss** mobility **grant** (€3k).

Bachelor in Informatics Engineering

Sep 2013 – July 2017

Polytechnic University of Catalonia (UPC) · Specialisation in Computer Engineering *GPA: 7.65/10*

Experience (Academia & Industry)

Postdoctoral Researcher & Research Lead

July 2025 – Present

Barcelona Supercomputing Center (BSC) *Barcelona, Spain*

- **Managing the research agenda** for a team of 4 (BSc, MSc, PhD, RE), and coordinating international collaborations with **UCSB** and **PoliMilano**.
- **Leading** the integration of Metro-MPI into **Verilator** and large-scale **multi-FPGA environments**, and **designing SpMV accelerators** in RTL.
- **Driving** research on **LLM-based**, **agent**-driven **hardware design** workflows to automate RTL generation and hardware-software co-design.

PhD Researcher

May 2021 – July 2025

Barcelona Supercomputing Center (BSC) *Barcelona, Spain*

- **Designed Data Centre HyperLoops (DHL):** Developed a novel communication solution that achieves **114**× to **646**× **faster data movement** compared to standard 400 Gbps optical networks for ML workloads in hyperscale environments (**ISCA '24**).
- **Scaled RTL Simulation (Metro-MPI)**: Engineered a distributed simulation framework that scaled to **1,024** cores with a **134**× **speedup**, enabling the simulation of billion-transistor SoCs that were previously computationally prohibitive (**DATE '23**).
- **Open-Source Hardware Leadership**: Implemented **MPMC queue-based accelerator interfaces** (RTL and C libraries) with **coherent memory subsystems**, enabling cleaner and more scalable accelerator integration across multiple RISC-V designs (under review).
- **Collaborations** with **EU projects**: EPI, DRAC, MEEP; **Industry**: Arm CoE, Intel; **Academia**: UCSB, and HM.

Google Summer of Code — Mentor & Student

Summer of 2018, 2021, 2025

Google Summer of Code *Remote*

- **Mentor** (2025, **FOSSi**): Mentored the automation of **Metro-MPI** into open-source manycore simulation workflows.
- **Student** (2021, **FOSSi**): Parallelised **RTL simulations using MPI**, scaling to 1024 cores with **134**× **speedup** (***DATE '23***).
- **Student** (2018, **PCP**): Developed **production** features for **Performance Co-Pilot (PCP)**, enabling efficient agent-to-agent data transmissions.

Research Master Student *March 2018 – April 2021*

Barcelona Supercomputing Center (BSC) *Barcelona, Spain*

- **MSc Thesis**: *Towards the Simulation and Emulation of Large-Scale Hardware Designs.*
- Designed **gem5+RTL Framework (ICPP '21)**, enabling co-simulation of RTL models within a complete software stack.
- **Engineered NoC tracing** for MontBlanc 2020, enabling performance analysis of **Exascale-ready systems** (***DATE '21***).
- **Awarded the Nacho Navarro Grant**, given to the top-performing 2 students in the High-Performance Computing (HPC) track.

Intern at XLABS (Research & Product Team) *Aug 2017 – Feb 2018*

Xilinx (now AMD) *Dublin, Ireland*

- **Performance Analysis**: Evaluated the scalability of the **ACAP accelerator** to identify bottlenecks in the next-generation FPGA architecture.
- **Infrastructure Reliability**: Owned and maintained critical components of the **nightly regression testing** for the accelerator simulator.

Undergraduate Researcher (EU Project RoMoL) *July 2016 – Feb 2017*

Barcelona Supercomputing Center (BSC) *Barcelona, Spain*

- **BSc Thesis**: Integrated the **Ramulator** memory simulator into the trace-driven simulator **TaskSim**.
- ***Awarded*** *the prestigious Spanish Ministry* ***Beca de Colaboración*** *(€2,000) for undergraduate research.*

Invited Talks

2025	**Past, Present and Future of Designing, Integrating and Simulating RTL Models,** Invited Seminar	*PoliMilano*
2023	**Exascale Simulation of Next-Generation Computing Architectures,** Invited Workshop Talk	*IISWC*

Publications

2025	**First Author Paper,** *Advanced Communications Patterns Support for Hardware Accelerators*	*(under review)*
2024	**Co-First Author Paper,** *The Case For Data Centre HyperLoops*	***ISCA '24***
2023	**First Author Paper,** Characterization of a Coherent Hardware Accelerator Framework for SoCs	***Samos '23***
2023	**First Author Paper,** Fast Behavioural RTL Simulation of 10B Transistor SoC Designs with Metro-MPI	***DATE '23***
2021	**First Author Paper,** gem5+rtl: A Framework to Enable RTL Models Inside a Full-System Simulator	***ICPP '21***
	Co-Author Papers, NoCArc '23, DSD '22, DATE '21, DCIS '23/'21, FGCS '24 and JETCAS '24	*2019 – 2025*
	First Author Posters, at different venues: ACACES '21/'19, BSCDS '23, DAC '23, OSDA '24	*2019 – 2024*

Achievements

Professional Service & Community Leadership

- **PC**: ISCA '26, MICRO '26, CF '26, ASPLOS '26 & ISCA '26 AEC
- **External reviewer**: IPDPS '24, LATTE '24, ICPP '23, ICPP '22, DATE '21
- **Volunteer**: RISCV Summit '23/'19, FPL '19
- **Attendee**: ASPLOS '25, DATE '24/'23, IISWC '23, DAC '23, SAMOS '23, Arm Research Summit 2020

Communication Excellence: 2nd Place in "*PhD Thesis in 4 Minutes*" contest at UPC *2024*

Obtained competitive grants from undergrad, master, and PhD level (∼ €107,000) *2016 – current*

GSoC Student (twice), GSoC mentor, a competitive open-source initiative run by Google *2018 – 2025*

Hackathons & Start-Up Experience *2015 – 2021*

- Participated in 15+ hackathons, earning several distinctions, including the **GitHub Octocat Prize** (Edinburgh, 2018), **3rd place at Hack the Burgh** (Edinburgh, 2018), and finalist recognition at Copenhacks (Copenhagen, 2018).
- Electric bike start-up **Forestal**: lead the hardware-software integration between the bike and the mobile application.
- Accepted at the **most prestigious start-up programme** led by Santander Bank for undergraduates.

Involved in different associations during the Bachelor and Master *2016 – 2018*

- **HackUPC**: Help in the organisation of the biggest student Hackathon in Europe, as well as mentoring projects.

Skills

Hardware	**Tools**: gem5, Ramulator, Verilator, Vivado, ModelSim, VCS • **Design**: SystemVerilog, VHDL, HLS, FPGAs
Software	C/C++ (Expert), Python (NumPy, Matplotlib), OpenMP (Multithreading), MPI (Parallel Scaling), Linux Kernel/Drivers, GitLab CI/CD
Domains	Hyperscale Data Movement, Coherent Memory Systems, Hardware-Software Co-Design, SoC Integration, RISC-V, Accelerators
Interests	Climbing (max bouldering grade 8a/V11), skiing, mountaineering and table tennis (competed at the national level)

Languages

English Advanced Level (Duolingo 135/160) · **French** Basic Elementary Level (A1) · **Catalan** native · **Spanish** native